IN THE CLAIMS

Re-write Claims 39-40, 42-46, 51, 52, 54 and 55 as follows. Add new Claims 66 and 67 as follows. Cancel Claim 63.

1-38. (Cancelled)

39. (Currently Amended) An amplifier circuit comprising:

an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output; and

a power detector circuit including ~~at least~~ a first input and a second input, ~~inputs~~ each coupled to sample a signal transmitted along the signal path, wherein ~~at least~~ the first input is coupled to a first interior node of the signal path ~~at an interior node of the amplifier~~ and the second input is coupled to a second interior node of the signal path, the first and second interior nodes being ~~that is~~ disposed between, but ~~is~~ exclusive of, the input and the output of the amplifier, ~~and~~ wherein the power detector circuit is operable to sample the signal transmitted along the signal path at both the first and second interior nodes, thereby creating first and second sample signals, respectively, and combine the first and second sample signals to generate ~~output~~ a first signal reflective of both the first and second sample signals ~~the signal sampled at the at least first and second inputs,~~

~~wherein the second input of the power detector circuit is coupled to sample at a second interior node of the amplifier, the second interior node also being disposed between, but exclusive of, the input and the output of the amplifier.~~

40. (Currently Amended) The amplifier circuit of claim 39, wherein the plurality of amplifier stages comprises:

a first amplifier stage having an input connected to the input of the amplifier;

a final amplifier stage having an output connected to the output of the amplifier; and

~~further comprising~~ at least one intermediate ~~said~~ amplifier stage coupled between the first amplifier stage and the final amplifier stage in the signal path ~~between the first and second amplifiers~~,

wherein the first input is coupled for sampling between either the first amplifier stage and the at least one intermediate amplifier stage or between the at least one intermediate amplifier stage and the final amplifier stage.

41. (Cancelled)

42. (Currently Amended) The amplifier circuit of claim 40, wherein the amplifier comprises ~~a final said amplifier stage having an output, and~~ an output matching network having an input coupled to the output of the final amplifier stage and an output that forms the output of the amplifier.

43. (Currently Amended) The amplifier circuit of claim 39, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the first interior node is within the matching network.

44. (Currently Amended) The amplifier circuit of claim 39, further comprising a bias circuit, wherein the bias circuit provides a DC bias signal to at least one of the plurality of ~~first and second~~ amplifier stages, the bias signal depending, at least in part, on the first signal.

45. (Currently Amended) The amplifier circuit of claim 44, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the first interior node is within the matching network.

46. (Currently Amended) The amplifier circuit of claim 39, wherein the plurality of amplifier stages comprises a first amplifier stage having an input connected to the input of the amplifier, the amplifier circuit further comprising a bias circuit, wherein the bias circuit provides a variable bias signal to the first amplifier stage, the bias signal depending, at least in part, on the first signal.

47. (previously presented) The amplifier circuit of claim 39, wherein the first signal reflects a summing of signals derived from the sampling at the at least first and second inputs.

48. (previously presented) The amplifier circuit of claim 39, wherein the first signal reflects a difference between signals derived from the sampling at the at least first and second inputs.

49. (previously presented) The amplifier circuit of claim 39, wherein the first signal reflects a greater weight given to a signal derived from the sampling at one of the first and second inputs than to a signal derived from the sampling at other of the first and second inputs.

50. (previously presented) An amplifier circuit comprising:

an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output; and

a power detector circuit including at least first and second inputs each coupled to sample a signal, wherein the first and second inputs are each coupled to the signal path at first and second interior nodes, respectively, of the amplifier, the first and second interior nodes being disposed between, but exclusive of, the input and the output of the amplifier, and the power detector circuit is operable to output a first signal reflective of the signal sampled at the at least first and second inputs.

51. (Currently Amended) The amplifier circuit of claim 50, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the first interior node ~~comprises~~ is within the matching network.

52. (Currently Amended) The amplifier circuit of claim 50, wherein the plurality of amplifier stages comprises a first amplifier stage having an input coupled to the input of the amplifier, and a second amplifier stage having an input coupled to an output of the first amplifier

stage, the amplifier circuit further comprising a bias circuit, wherein the bias circuit provides a DC bias signal to at least one of the first and second amplifier stages, the bias signal depending, at least in part, on the first signal.

53. (previously presented) The amplifier circuit of claim 52, wherein the amplifier includes a matching network in the signal path within the amplifier and coupled between respective ones of the plurality of amplifier stages, wherein the first interior node is within the matching network.

54. (Currently Amended) The amplifier circuit of claim 50, wherein the plurality of amplifier stages comprises a first amplifier stage having an input connected to the input of the amplifier, the amplifier circuit further comprising a bias circuit, wherein the bias circuit provides a variable bias signal to the first amplifier stage, the bias signal depending, at least in part, on the first signal.

55. (Currently Amended) The amplifier circuit of claim 50, wherein the plurality of amplifier stages comprises a first amplifier stage having an input coupled to the input of the amplifier, and a second amplifier stage having an input coupled to an output of the first amplifier stage, the amplifier circuit further comprising a bias circuit, wherein the bias circuit provides a variable bias signal to the second amplifier stage, the bias signal depending, at least in part, on the first signal.

56. (previously presented) The amplifier circuit of claim 50, wherein the first signal reflects a summing of signals derived from the sampling at the at least first and second inputs.

57. (previously presented) The amplifier circuit of claim 50, wherein the first signal reflects a difference between signals derived from the sampling at the at least first and second inputs.

58. (previously presented) The amplifier circuit of claim 50, wherein the first signal reflects a greater weight given to a signal derived from the sampling at one of the first and second inputs than to a signal derived from the sampling at the other of the first and second inputs.

59. (Currently Amended) A method comprising:

providing an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output;

sampling a plurality of nodes, including sampling at an interior ~~said~~ node within the amplifier that is between, but exclusive of, the input and output of the amplifier;

forming a first signal reflective of the sampling at the plurality of nodes, including the interior ~~said~~ node;

providing a DC bias to at least one of the plurality amplifier stages, the DC bias being based, at least in part, on the first signal,

wherein the sampling includes sampling at a second interior ~~said~~ node on the signal path, the second interior ~~said~~ node being between, but exclusive of, the input and output of the amplifier.

60. (Cancelled)

61. (previously presented) The method of claim 59, wherein the first signal is formed by summing signals derived from the sampling.

62. (previously presented) The method of claim 59, wherein the first signal is formed based on a difference between signals derived from the sampling.

63. (Canceled) An amplifier circuit comprising:

an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output; and

a power detector circuit including at least first and second inputs each coupled to sample a signal, wherein at least the first input is coupled to the signal path at an interior node of the amplifier that is disposed between, but is exclusive of, the input and the output of the amplifier, and the power detector circuit is operable to output a first signal reflective of the signal sampled at the at least first and second inputs,

wherein the first signal reflects a difference between signals derived from the sampling at the at least first and second inputs.

64. (previously presented) A method comprising:

providing an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output;

sampling a plurality of nodes, including sampling at an interior said node within the amplifier that is between, but exclusive of, the input and output of the amplifier;

forming a first signal reflective of the sampling at the plurality of nodes, including the interior said node;

providing a DC bias to at least one of the plurality amplifier stages, the DC bias being based, at least in part, on the first signal,

wherein the first signal is formed by summing signals derived from the sampling.

65. (previously presented) A method comprising:

providing an amplifier comprising an input, an output, and a plurality of amplifier stages coupled in series between the input and the output, wherein a signal path extends through the plurality of amplifier stages between the input and the output;

sampling a plurality of nodes, including sampling at an interior said node within the amplifier that is between, but exclusive of, the input and output of the amplifier;

forming a first signal reflective of the sampling at the plurality of nodes, including the interior said node;

providing a DC bias to at least one of the plurality amplifier stages, the DC bias being based, at least in part, on the first signal,

wherein the first signal is formed based on a difference between signals derived from the sampling.

66. (New) The amplifier circuit of claim 50, wherein the plurality of amplifier stages comprises:

a first amplifier stage having an input connected to the input of the amplifier;

a final amplifier stage having an output connected to the output of the amplifier; and

at least one intermediate amplifier stage coupled between the first amplifier stage and the final amplifier stage in the signal path, wherein the first input is coupled for sampling between either the first amplifier stage and the at least one intermediate amplifier stage or between the at least one intermediate amplifier stage and the final amplifier stage.

67. (New) The amplifier circuit of claim 66, wherein the amplifier comprises an output matching network having an input coupled to the output of the final amplifier stage and an output that forms the output of the amplifier.